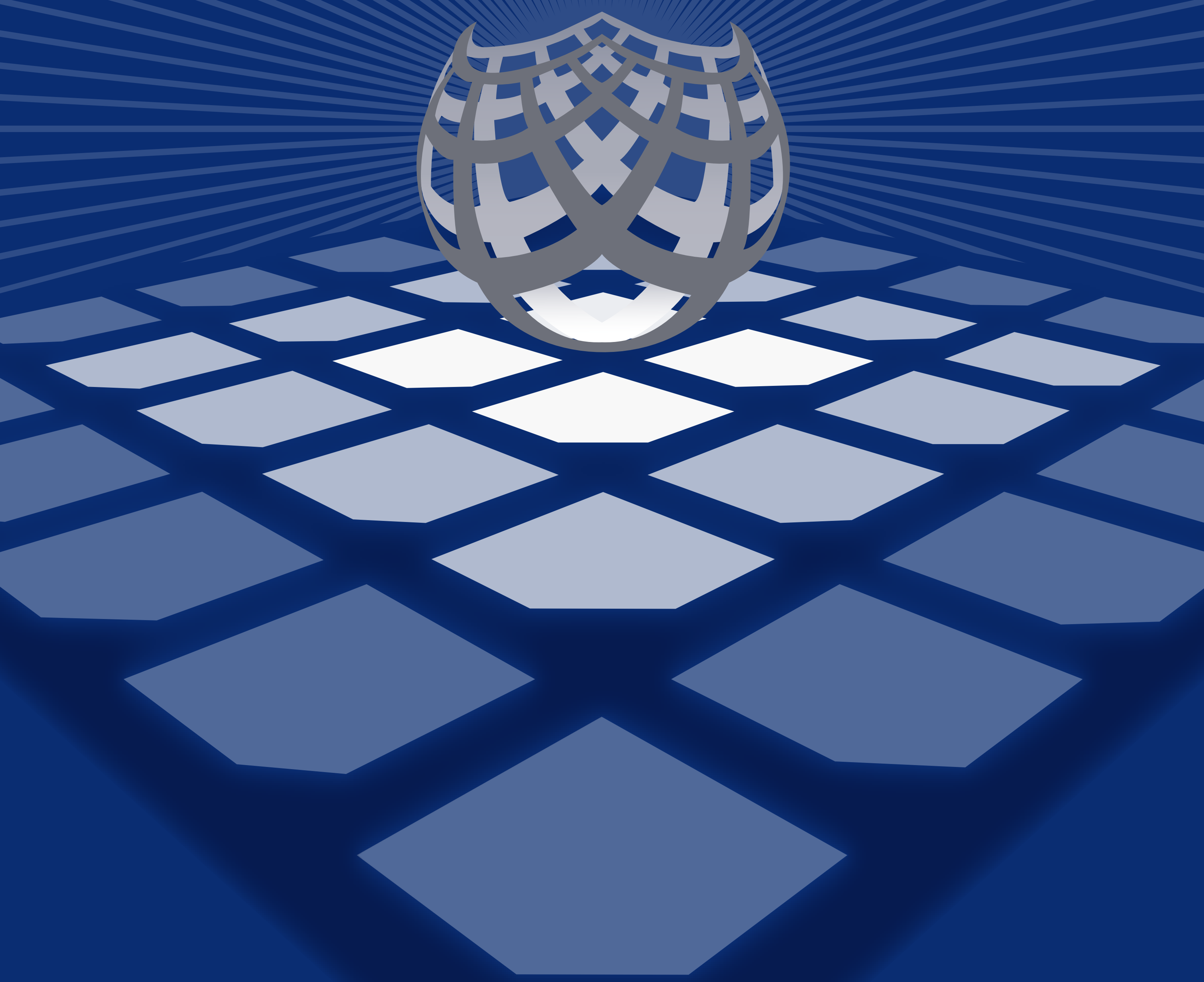
RISC-V
Collaboration, Scalability, and Innovation in Microprocessing



Telink

RISC-V: Collaboration, Scalability, and Innovation in Microprocessing

With the emergence of RISC-V, a free, open source instruction set architecture (ISA), a new era of processing characterized by customizability and innovation is on the horizon. In the ever-expanding realm of semiconductors, open source processing has the potential to kickstart innovation, reduce costs, and improve developers' access to better performance and functionality.

As an open source ISA, RISC-V not only facilitates more innovative and secure processor design, but offers developers a depth of design knowledge that has hitherto been prohibitively expensive for all but Fortune 50 companies. As such, anyone working in device manufacturing, system architecture, electronics design, or even software development — possibly even those working in procurement or component supply chain — should consider how RISC-V might be able to help them improve the design and roadmap planning of their products.

Initially created at the University of California, Berkeley in 2010, RISC-V was pushed into commercial use in 2015 with the creation of the non-profit RISC-V Foundation. The 325-plus members of the foundation are able to participate in the development of the RISC-V ISA and extensions, and guide their evolution.

Backed by the foundation's Board of Directors — which includes industry leaders like Google, Western Digital, and NVIDIA — RISC-V has the potential to improve processor functionality and reduce the cost of computer systems. RISC-V is not as scale-dependant as most ISAs, meaning it can be implemented in hardware ranging from MCUs to large server cores. Telink plans to bring RISC-V to market starting with highly specialized computational devices (think: the IoT).

As of June 2019, Version 2.2 of the RISC-V user-space ISA and Version 1.11 of the RISC-V privileged ISA are frozen, meaning real-world software and hardware development can proceed, a fact about which we at Telink are incredibly excited.

An Overview of ISAs

To fully grasp the scope of RISC-V's potential, one must first develop an understanding of how instruction set architectures affect the creation of processors and computers more generally.

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Defining ISAs

In short, an ISA is an abstraction of a computer. At the most basic level, it's the language a processor uses to interpret and execute instructions that are sent from an operating system or software program. In addition to handling programmatic functions, ISAs can help processors execute other important tasks like software and hardware interrupt handling, memory addressing, supported data type definition, and input/output management.

In modern computers — especially smartphones and other IoT devices — processors sit on the same physical chips as other important system components. Therefore, beyond acting as a processor's "language," an ISA must define how the processor interacts with the rest of the components on a chip.

The Shortcomings of Proprietary ISAs

Software that has been written for an ISA can run on different implementations of the same ISA, and in theory, this allows for binary compatibility between different generations of chips and devices. This means that if several chips are part of the same family, software will be portable between them.

As an example, consider Intel's x86 line of processors. The line has existed for 40 years, and this longevity has given developers the chance to document and maintain code for many different machines as they've continued to develop the x86 architecture. While this is great for a developer who has a long history of using Intel chips, what if the chips stop meeting the developer's needs?

Such a shift in needs can be precipitated by a variety of factors — a budgetary change, a pivot to building devices that need more or less processing power, etc. — and in these situations, developers are unable to port code from their current chips to a new vendor's chips. This can render years of software development practically unusable overnight. This is a major issue in the current ISA market, but it isn't the only issue — nor is it the biggest.

Due to their complexity, ISAs are expensive to design and maintain, and as a result, the market is filled with proprietary ISAs like Intel's x86 and ARM's Cortex-M series that are licensed to chip companies for potentially significant fees. Intel's lack of licensing has limited competitive entrants to the market, whereas ARM's costly licensing has frustrated entrants looking for an ISA with extensibility or enhancements. As a result, for the past several decades, the power to drive ISA innovation has been concentrated in the hands of a fairly small group of people. This is changing thanks to the ongoing rollout of RISC-V.

An Open Source Alternative

As an open source alternative to proprietary ISAs, RISC-V ensures chip companies need no longer wonder why ISAs are designed the way they are. By utilizing RISC-V, companies gain full access to their ISA's design, are able to easily understand why it works the way it does, and can use this knowledge to inform their hardware production. And since RISC-V is open source, companies need not pay big-ticket fees to obtain this depth of insight — everything is readily available. This levels the playing field of processor innovation in a powerful way.

Indeed, thanks to the open, collaborative spirit that underlies the entire RISC-V project, companies looking to pioneer new technologies by leveraging ISAs don't need to do so alone. Members of the RISC-V Foundation vote on updates to the ISA, work with companies across the globe, and receive support from the Linux Foundation in the form of training programs, infrastructure tools, and more.

Developers that work with RISC-V gain an understanding of "the why" behind the ISA, and can even influence its development, which enables them to maximize the value they derive from both current and future iterations of the architecture.

The Open Source Roadmap

Taking a step back, economic theory dictates that, no matter the product or industry in question, the market always demands alternatives. In the context of software development, this alternative has often come from open source technologies and movements. While there are undoubtedly reasons and needs for competitive proprietary technologies, competitive open source technologies often make a broader and deeper industry impact.

There have been numerous open source projects that have led to the creation of exemplary products. For example, Linux, an open source operating system kernel, is one of the most popular and widely-used open source technologies. Although it started as a personal project in 1991, Linux has evolved into the de facto operating system of choice for supercomputers, web servers, and various devices across industries — and is now even being used by the International Space Station.

Similarly, since its launch in 1995, the open source Apache HTTP Server has become the most popular web server on the Internet — as of 2019, it services nearly 29 percent of all active websites. Even Chromebooks (which run on the Linux kernel) have made serious waves in the laptop industry. In fact, when Google unveiled its line of devices that ran Chrome OS, they outsold MacBooks in the United States.

These products showcase the immense collaborative potential of an open source approach, which allows people from around the globe to work together, share ideas, and contribute to projects in a meaningful way. Without having to worry about proprietary licensing or adhering to nondisclosure agreements, an array of companies — even competitors — are able to work together on the same technologies and bring their unique perspectives to the table.

The fact that RISC-V is open source means that it offers many of the same benefits as these other open source technologies. Anyone can work on and collaborate around RISC-V, meaning developers of all stripes can optimize chips, frameworks, and software for the community at large. Generally speaking, an open source approach makes for a bigger, more diverse developer and manufacturer community; one with more open conversations that can improve how we design, build, and connect our devices.

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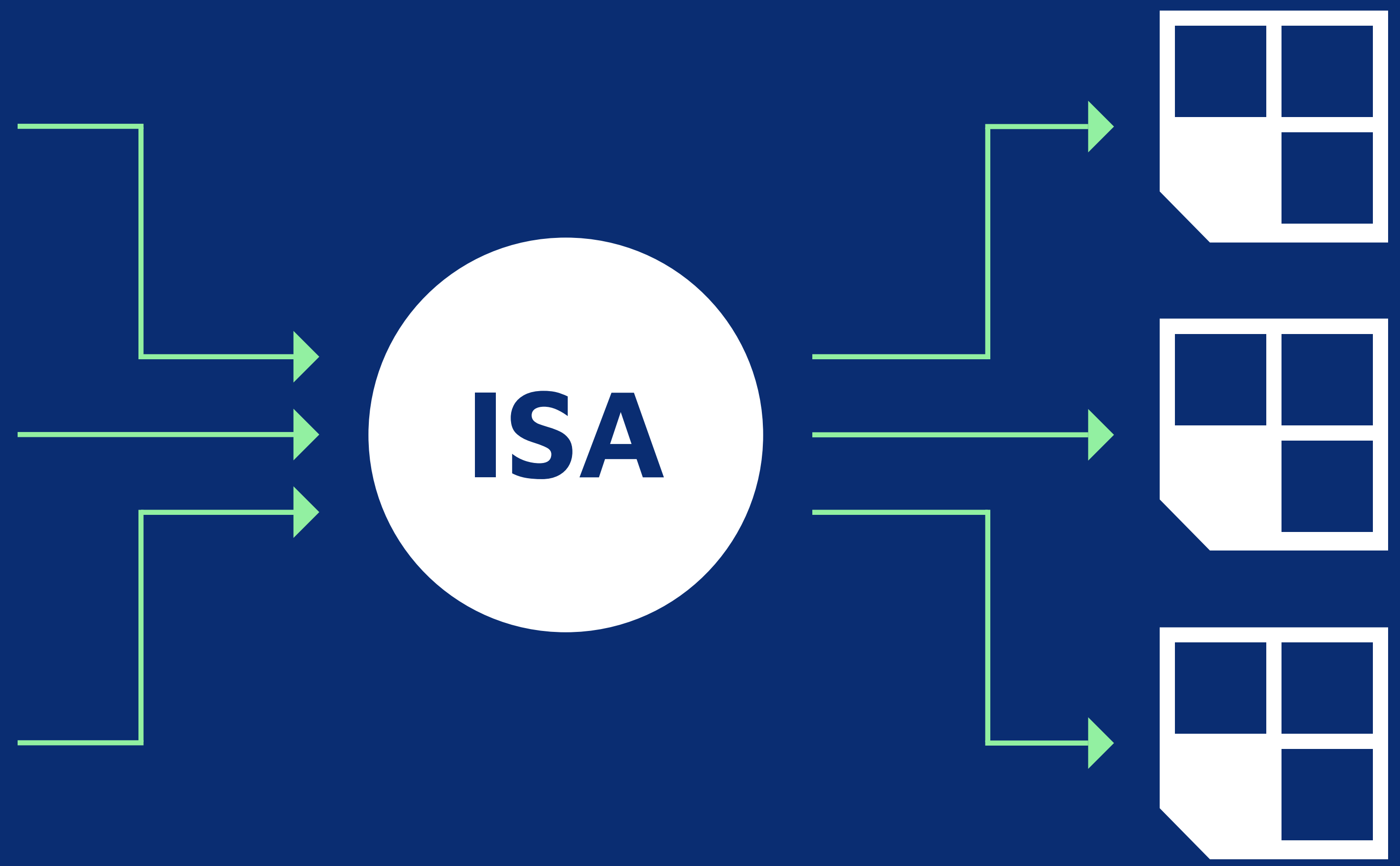

RISC-V also saves developers the headache of having to write new code just because they want to change chip vendors. With the ability to port code from one RISC-V platform into another RISC-V platform, developers won't be stuck with the sunk costs they have experienced as a result of switching between proprietary ISA vendors.

Just as this portability provides integrated circuit companies with a path to scaling into adjacent markets based on capability or performance, it provides a path to developers and device-makers to do the same. Imagine you're a manufacturer of MCUs for commodity consumer electronics. RISC-V would enable you to, for instance, address application processors in data center products without having to develop for an entirely different ISA. Granted, there's more to products than their ISAs, but the flexibility RISC-V provides eliminates a nontrivial hurdle for developers.

If the Linuxes, Apaches, and Chromebooks of the world are any indication of how the tech community responds to open source alternatives, it's fair to assume that once RISC-V finds its way into the market in earnest, major companies will begin leveraging it to drive processor innovation in ways that simply haven't been possible until now.

The Tangible Benefits of RISC-V for MCUs

Open source licensing has long been the engine driving breakneck technological advances. The speed and functionality of software, however, is bound by the architecture of the processors running it. On the whole, this hardware has yet to reap the benefits that open source has to offer to the same extent as software has, but this is starting to change as RISC-V sets a new standard for what developers can achieve. The question now is, "What is the scale of creative transformation that this openness will unleash?"

Returning to proprietary ISAs, there are two dominant architectures in the market. Intel Architecture (x86) is pervasive in general purpose computers and data centers (where high performance is of the utmost importance), whereas ARM's architecture is favored for 32-bit MCUs in high-end mobile devices and smartphones.

If developers, designers, and architects want more from these proprietary architectures — more flexibility, more extensibility, better performance — they have little choice but to wait until the architectures' owners decide to make changes. Further, even once these owners decide to make such changes, developers, designers, and architects must wait until licensees of the proprietary architectures adopt these changes, test and manufacture them, and release updated software development tools before they will be able to realize their goals.

While this process must still happen with RISC-V platforms, the critical first step — ISA-level changes — can now be advanced by all, even in multiple directions. Indeed, RISC-V enables manufacturers to produce low-power MCUs, high-power MCUs, compute-intensive designs, and more while maintaining binary portability. So while ARM's proprietary ISA needs to be extended to deliver the necessary capabilities for domains that have traditionally fallen outside its domain and Intel's proprietary ISA needs to be extended to deliver the necessary capabilities for very low-power, low-compute devices, the RISC-V ISA can easily be scaled to address any and all market needs.

Telink currently makes efficient, low-power SoCs, so we're focused on MCUs. While we've aimed to deliver the smallest, most efficient cores for a large spectrum of applications, we recognize that bringing reliable connectivity to increasingly complex devices with higher compute demands will require maximum scalability and flexibility to extend features and support in multiple directions.

While our proprietary ISA is able to deliver efficiency and ultra-low power consumption, increasing its compute would require significant resources. Supplementing our suite of offerings with a widely-used proprietary ISA would ensure our developers aren't beholden to a single architecture target, but adopting RISC-V would do the same while incorporating the innovation inherent in open source approaches. For example, the RISC-V AndesCore D25F performs at 2.85 DMIPS/MHz or 3.58 CoreMark/MHz, which compares favorably to most ARM Cortex M4F designs.

> **By embracing RISC-V now, we're taking an open, community-based approach to addressing an even wider audience.**

There are already many competitive solutions that offer high-performance, high-extensibility, feature-rich core designs. This enables us to pick the right blocks for our SoCs and even deliver better performance than similar ARM-based offerings, allowing us to focus our optimization and integration on other key components — such as our software protocol stacks and radio performance — and provide a common toolchain and interfaces that deliver better portability and familiarity for developers.

Today, if you were to use Telink chips in end nodes, ARM chips in gateways, and Intel chips in workstations, you would be faced with three very different chip architectures that only complicate an already diverse device target. In the future, a customer using Telink SoCs for low-power connectivity could use other RISC-V-based solutions for other devices, creating a more common and unified development base.

Telink and the Future of RISC-V

At Telink, our mission is to bring the ideal platforms for IoT to market — high performance, high reliability, and maximum flexibility at affordable prices across the spectrum. We offer more flexibility and better solutions for all developers, from garage startups to Fortune 50s.

We're proud to have pioneered Bluetooth Mesh and multi-protocol SoCs, and we're excitedly looking forward to the RISC-V era of solutions from Telink. Our proprietary MCUs have filled — and continue to fill — a market gap in efficient, low-cost solutions. By embracing RISC-V now, we're taking an open, community-based approach to addressing an even wider audience, facilitating advances and improvements all along our tool-chain. As we expand our technology and platform roadmap, you will be able to continue to rely on the same stability in our tools that you'd expect from the RISC-V Foundation and its members.

Bluetooth Mesh and multi-protocol have continued to move toward de facto status in the IoT space, and we believe that RISC-V will have a similar level of influence. The benefits of RISC-V will make an immediate impact for developers, designers, architects, and end users. Meanwhile, the RISC-V community's investments in innovation will deliver profound and enduring technological returns.

The Front Cover Explained:

The cover depicts a stereographic projection of a sphere onto a two-dimensional surface. Light shines through the spherical object such that it throws a regular pattern onto the plane. We were inspired to use this visualization as a way to depict how the RISC-V ISA can define a diversity of implementations.

Contact

telink-semi.com

+1 (408) 320-2197

sales@telink-semi.com

Telink